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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/791,216 | 03/02/2004 | Daniel Lambright | EMS-00503 | 3938 |

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Patent Group
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| EXAMINER | |
|---|---|
| NGUYEN, HIEP T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | |

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/791,216 | LAMBRIGHT ET AL. | |
| | Examiner | Art Unit | |
| | Hiep T Nguyen | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *31-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is a response to the preliminary amendment filed June 30, 2004. Claims 31-62 are pending in the application. Applicant has canceled claims 1-30.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 31-62 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,728,836. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed invention in the instant claims 31-62 is no more than an obvious variation of that in the patented claims 1-18.

   a. <u>As per claim 1:</u>

      i. The patented claim 1 teaches the three claimed steps of "apportioning the cache..." and "providing a first segment ..." and "providing a second segment ..." [see the patented claim 1, lines 1-34].

      ii. The patented claim 1, however, does not teach the steps of removing a block of cache memory from one of said first and said second segment; and returning the block to an assigned segments wherein said assigned segment is one of the other of said first and said second segments, a same segment from which said block was removed, and a randomly assigned segment.

iii. One having ordinary skill in the art at the time the invention was made would readily recognize that the two claimed steps of "removing" and "returning" are no more than the operations of dynamic allocation cache space into plurality of cache segments. Caches partitioning into a plurality of segments and dynamically assigning cache blocks among segments have been known and widely practice in the pertinent art for the purpose of maximize the cache space utilization.

iv. One having ordinary skill in the art, who is familiar with such dynamic cache allocation, looks at the teaching of the patented claim 1, would lead he or she to further incorporate the dynamic cache allocation teaching into the method of storing data in a cache of the patented claim 1 so as to further improve and/or maximize the cache space usage.

v. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further includes the steps of removing a block of cache memory from one of said first and said second segment; and returning the block to an assigned segments wherein said assigned segment is one of the other of said first and said second segments, a same segment from which said block was removed, and a randomly assigned segment into the method of the patented claim 1.

vi. The ability to improve and/or maximize the cache space usage provides sufficient suggestion and motivation to one having ordinary skill in the art to do such steps employment in the method of the patented claim 1.

b. As per clams 32-40:thefurther claimed limitations are either explicitly or implicitly taught by that in claims 2-9 of the patent.

c. As per claims 41-47:

i. Claims 10-15 of the patent teaches each and every clamed limitations in the instant claims 41-47, except the claimed limitation of "wherein a host is included

in one of said first plurality and said second plurality in accordance with criteria including at least one of :access to a predetermined amount of said cache, a priority level, and a level of service.

ii. Again, assigning a cache segment to processing entity based on a priority level or access frequency [access to a predetermined amount of said cache] or hit density [a level of service] have also been known and widely practiced in the pertinent art.

iii. It would have been obvious to one having ordinary skill in the art a the time the invention was made to group the processors in accordance with criteria including at least one of :access to a predetermined amount of said cache, a priority level, and a level of service so as to further improve the system performance, as well known..

d. As per claims 48-51:

i. Claim 16 of the patent does not teach the limitation of "each of said first and second segments being accessible simultaneously by different processors.

ii. Partitioning a cache into a plurality of cache segments for the purpose of parallel or simultaneous accessed by different processors ahs also been known and widely practiced in the pertinent art. The advantage of parallel accessing comparing to serially accessing would readily recognize by one having ordinary skill in the art.

iii. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to configure the cache segments of the patented claim 16 to allow parallel accessing to the cache segments by different processors.

e. As per claim 52-54:

i. The patented claims 17-18 does not teach the claimed limitations of "wherein the block of cache memory that is provided is at least one of :a next available block,

a block corresponding to a plurality of external host systems having a greatest number of blocks assigned thereto, a block corresponding to a plurality of external host systems having a greatest number of available blocks, and a block corresponding to a plurality of external host systems having a greatest percentage of available blocks. Still, each of the mentioned cache block allocation and/or assignment has been known and commonly practiced in the pertinent art. It would have been obvious to one having ordinary skill in the art to select one of the commonly practiced cache block assignment or allocation to be implemented into the system of patented claims 17-18.

f. As per claim 55: each and every claimed limitations is taught by that in either one of the patented independent claims of he patent.

g. As per claims 56-62, similarly to claims 41-47, it would have been obvious o one having ordinary skill in the art at the time the invention was made to assign a number of cache slots in each segment in accordance with particular criteria associated with each segment.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T Nguyen whose telephone number is (703) 305-3822. The examiner can normally be reached on Monday-Friday from 9:30 a.m. to 6:00 p.m.
5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep T Nguyen
Primary Examiner
Art Unit 2187

HTN